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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LEWIS, DAVID LEE	
ART UNIT	**PAPER NUMBER**
2629	

DATE MAILED: 11/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,805	PARK ET AL.	
	Examiner	Art Unit	
	David L. Lewis	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. **Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moon (2003/0043100).**

As in claim 1, Moon teaches of a liquid crystal display, **figure 4, paragraph 2,**

comprising: a liquid crystal panel including a plurality of pixels including switching elements, **figure 4 item 100, paragraph 31, 53,**

a plurality of gate lines for transmitting gate signals to the switching elements, **figure 4 item 111, paragraph 31**

and a plurality of data lines for transmitting data voltages to the pixels, **figure 4 item 112, paragraph 31;**

a data driver including a plurality of data driving ICs connected to respective sets of the data lines, receiving image data, and applying the data voltages corresponding to the image data to the data lines, **figures 1-4 item 3;**

and a gate driver applying the gate signals to the gate lines, **figure 1 item 2**

wherein the data driving ICs are supplied with , a ground voltage and a supply voltage, **paragraph 57, figure 3 item 3 (Vdd, Gnd), figure 1 item 4, paragraph 31, wherein Vcom voltage as a reference voltage for the TFT's is provided.**

and voltage levels of the image data swing with reference to a reference voltage lower than the supply voltage, **paragraph 19, 62**. Wherein low voltage differential signaling and reduced swing differential signaling are performed which are equivalent to said feature as is known.

However Moon is silent as to the data driving ICs explicitly being supplied with a reference voltage. The specific term reference voltage is not used however Moon obviously provides for said reference voltage in view of voltage generator 6 providing gray voltage.

Said reference voltage would have been obvious to the skilled artisan in view of Moon' teaching of a first and second low voltage differential signals (LVDS) or reduced swing differential signals (RSDS), paragraph 19. Wherein such a driving configuration produces a positive and negative voltage swing around a reference voltage value at or other than ground. For example if the reference voltage is 0.5, the swing differential can be 2.5 (plus and minus the reference voltage), making the swing between –2.0 and 3.0 volts. If the reference voltage is 2.5, the swing differential of 2.5 will provided for a swing between 0 and 5 volts. Moon includes voltage generators 4 and 6 that obviously supply a reference value to accommodate the embodiment featuring LVDS. Therefore in order to produce a data driving IC capable of LVDS, the data driving IC's would require being supplied with a reference voltage for the purpose of said LVDS. The Voltage generator 6 supplies a reference voltage.

Therefore it would have been obvious to the skilled artisan at the time of the invention to provide for a reference voltage from a voltage generator 6 as

supplied by Moon because Moon teaching of an embodiment featuring LVDS that would require a reference voltage as claimed.

As in claim 2, Moon teaches of wherein the data driving ICs are mounted on the liquid crystal panel, paragraph 34.

As in claim 3, Moon teaches of wherein the image data received by the data driver are first inputted into at least one of the data driving ICs and shifted to other data driving ICs. paragraph 38-40, 57

As in claim 4, Moon teaches of wherein the data driving ICs include first and second sets of data driving ICs, figure 4 items 3k and 3k+1, and the image data include first and second image data to be inputted into the first and the second sets of data driving ICs, respectively, figure 4 item F2, paragraph 53.

As in claim 5, Moon teaches of wherein each of the first and the second sets of data driving ICs includes one data driving IC receiving the image data from an external device, figure 4 items 3k and 3k+1, paragraph 55-57.

As in claim 6, Moon teaches of wherein the image data for a data driving IC farther from the one data driving IC receiving the image data from the external device precede the image data for a data driving IC closer to the one data driving IC receiving the image data from the external device, figure 4 items 31 and 3k, paragraph 55-57.

As in claim 7, Moon teaches of further comprising a voltage generator for generating the reference voltage to be provided for the data driver and for generating voltages required for the gate signals to be provided for the gate driver, figure 1 item 4, paragraph 31.

As in claim 8, Moon teaches of wherein the voltage generator generates a plurality of gray voltages to be supplied to the data driver and to be selected as the data voltages, figure 1 item 4, paragraph 31.

As in claim 9, Moon teaches of wherein the reference voltage is inputted to the data driving ICs simultaneously, figure 3 items 3, paragraph 39-40.

As in claim 10, Moon teaches of wherein a signal line for transmitting the reference voltage is provided on the liquid crystal panel, paragraph 40.

As in claim 11, Moon teaches of wherein the image data have a voltage swing level lower than a voltage swing level of a signal transmitted in TTL/CMOS (transistor-transistor logic/complementary metal oxide semiconductor) transmission, paragraph 19 and 62. Wherein said feature is equivalent to LVDS as known in the art, wherein the examiner serves official notice that the LVDS swings are one tenth of the traditional TTL/CMOS levels.

As in claim 12, Moon teaches of wherein the gate driver includes a plurality of gate driving ICs connected to respective sets of gate lines, figure 4 item 2, paragraph 54.

As in claim 13, Moon teaches of a method of driving a liquid crystal display, **figure 1-4,**

including a liquid crystal panel having a plurality of pixels, **figure 1 item 1, figure 4 item 100,**

a plurality of gate lines, **figure 4 item 111,**

and a plurality of data lines, **figure 4 item 112,**

a data driver including a plurality of data driving ICs for supplying data voltages to the data lines, **figures 1-4 item 3**

and a gate driver for supplying gate signals to the gate lines, **figure 1 item 2,**

the method comprising: inputting the image data to at least one of the data driving ICs, **figure 4 item F2, paragraph 55;**

and shifting the image data to the data driving ICs, **paragraph 38-40, 57**

wherein the data driving ICs are supplied with a ground voltage and a supply voltage, **paragraph 57, figure 3 item 3 (Vdd, Gnd)**

and voltage levels of the image data swing with reference to a reference voltage lower than the supply voltage, **paragraph 19, 62**. Wherein low voltage differential signaling and reduced swing differential signaling are performed which are equivalent to said feature as is known.

However Moon is silent as to the data driving ICs explicitly being supplied with a reference voltage. The specific term reference voltage is not used however Moon obviously provides for said reference voltage in view of voltage generator 6 providing gray voltage.

Said reference voltage would have been obvious to the skilled artisan in view of Moon' teaching of a first and second low voltage differential signals (LVDS) or reduced swing differential signals (RSDS), paragraph 19. Wherein such a driving configuration produces a positive and negative voltage swing around a reference voltage value at or other than ground. For example if the reference voltage is 0.5, the swing differential can be 2.5 (plus and minus the reference voltage),

making the swing between –2.0 and 3.0 volts. If the reference voltage is 2.5, the swing differential of 2.5 will provided for a swing between 0 and 5 volts. Moon includes voltage generators 4 and 6 that obviously supply a reference value to accommodate the embodiment featuring LVDS. Therefore in order to produce a data driving IC capable of LVDS, the data driving IC's would require being supplied with a reference voltage for the purpose of said LVDS. The Voltage generator 6 supplies a reference voltage.

Therefore it would have been obvious to the skilled artisan at the time of the invention to provide for a reference voltage from a voltage generator 6 as supplied by Moon because Moon teaching of an embodiment featuring LVDS that would require a reference voltage as claimed.

As in claim 14, Moon teaches of wherein the shift direction of the image data is two, figure 4 items 3k and 3k+1, paragraph 55-57.

As in claim 15, Moon teaches of wherein the image data has a voltage swing level lower than a voltage swing level of a signal transmitted in TTL/CMOS (transistor-transistor logic/complementary metal oxide semiconductor) transmission, paragraph 19 and 62. Wherein said feature is equivalent to LVDS as known in the art, wherein the examiner serves official notice that the LVDS swings are one tenth of the traditional TTL/CMOS levels.

As in claim 16, Moon teaches of wherein the reference voltage is simultaneously inputted to the data driving ICs, figure 3 items 3, paragraph 39-40.

Response to Arguments

2. Applicant's arguments filed 9/5/2006 have been fully considered but they are not persuasive. Moon teaches of LVDS which includes a voltage swing around a reference voltage as known in the art of the LVDS standard. The swing is around the reference voltage by a voltage value less than the conventional supply voltage values. Therefore said reference voltage feature is obviously within Moon's teaching of LVDS wherein the gray voltage generator 6 provides for said reference voltage. Rejection Maintained.

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **David L. Lewis** whose telephone number is **(571) 272-7673**. The examiner can normally be reached on MT and THF from 8 to 5. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached on **(571) 272-7681**. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571)-273-8300.

5. Please note that all future correspondences directed to David L. Lewis must be sent to Art Unit 2629.

6. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner: David L. Lewis
November 22, 2006

BIPIN SHALWALA
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600